Embedded Systems

Ch 13B
Analog Interface & Codec

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Overview

- 1. Introduction
- 2. A/D Conversion
- 3. ADC Interface
- 4. Sensor Interface
- 5. D/A Conversion
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- 7. Codec
- 8. ACUNIT in Xscale
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7. Codec

- **Codec**
  - Coder-DECoder
  - Both ADC and DAC are supported
  - Usually coupled with the algorithm that is used to perform the coding

- Codecs
  - Linear
    - Standard ADC and DAC
    - Relationship between analog input and digital representation is linea
    - Frequently used for digital audio
  - A-law and u-law
    - Telecommunication applications with a limited bandwidth of 300 to 3100 Hz
    - Logarithmic cocdec with 8 bit samples at 8 kHz
    - A-law in UK, u-law in US
    - Conversion using look-up table

Codec (II)

- Codecs (Cont'd)
  - PCM (Pulse Code Modulation)
    - Represent the analog signal by a series of pulses whose amplitude is determined by the digital value.
    - Frequently used in telecommunication industry
  - DPCM (Differential PCM)
    - The value encoded is the difference between the current sample and the previous sample.
    - Can improve accuracy and resolution
    - The change in the analog value from one sample to another must be less than the differential range, and this determines the maximum slope of any waveform that is encoded.
  - ADPCM (Adaptive DPCM)
    - Some bits are used to encode the quantization value that was used to encode the data
    - The resolution of the difference can be adjusted (adapted) as needed.
    - Better resolution and dynamic range.

8. ACUNIT in Xscale

- **The AC'97 Controller Unit (ACUNIT) of the PXA255 processor**
  - Supports the AC'97 revision 2.0 features.
  - Supports audio controller link (AC-link)
    - AC-link: a serial interface for transferring digital audio, modem, mic-in, CODEC register control, and status information.
  - The AC'97 CODEC sends the digitized audio samples that the ACUNIT stores in memory.
    - For playback or synthesized audio production, the processor retrieves stored audio samples and sends them to the CODEC through the AC-link.
    - The external digital-to-analog converter (DAC) in the CODEC then converts the audio samples to an analog audio waveform.
  - ***Note:*** The ACUNIT and the I2S Controller cannot be used at the same time.

ACUNIT in Xscale (II)

- **Features supported:**
  - Independent channels for stereo Pulse Code Modulated (PCM) In, Stereo PCM Out, modem-out, modem-in, and mono mic-in.

    All of the above channels support only 16-bit samples in hardware.

    Samples less than 16 bits are supported through software.
  - Multiple sample rate AC'97 2.0 CODECs (48 kHz and below).

    The ACUNIT depends on the CODEC to control the varying rate.
  - Read/write access to AC'97 registers.
  - Secondary CODEC support.
  - Three Receive FIFOs (32-bit, 16 entries).
  - Two Transmit FIFOs (32-bit, 16 entries).
- **Features not supported:**
  - Double-rate sampling (n+1 sample for PCM L, R & C)
  - 18- and 20-bit sample lengths.

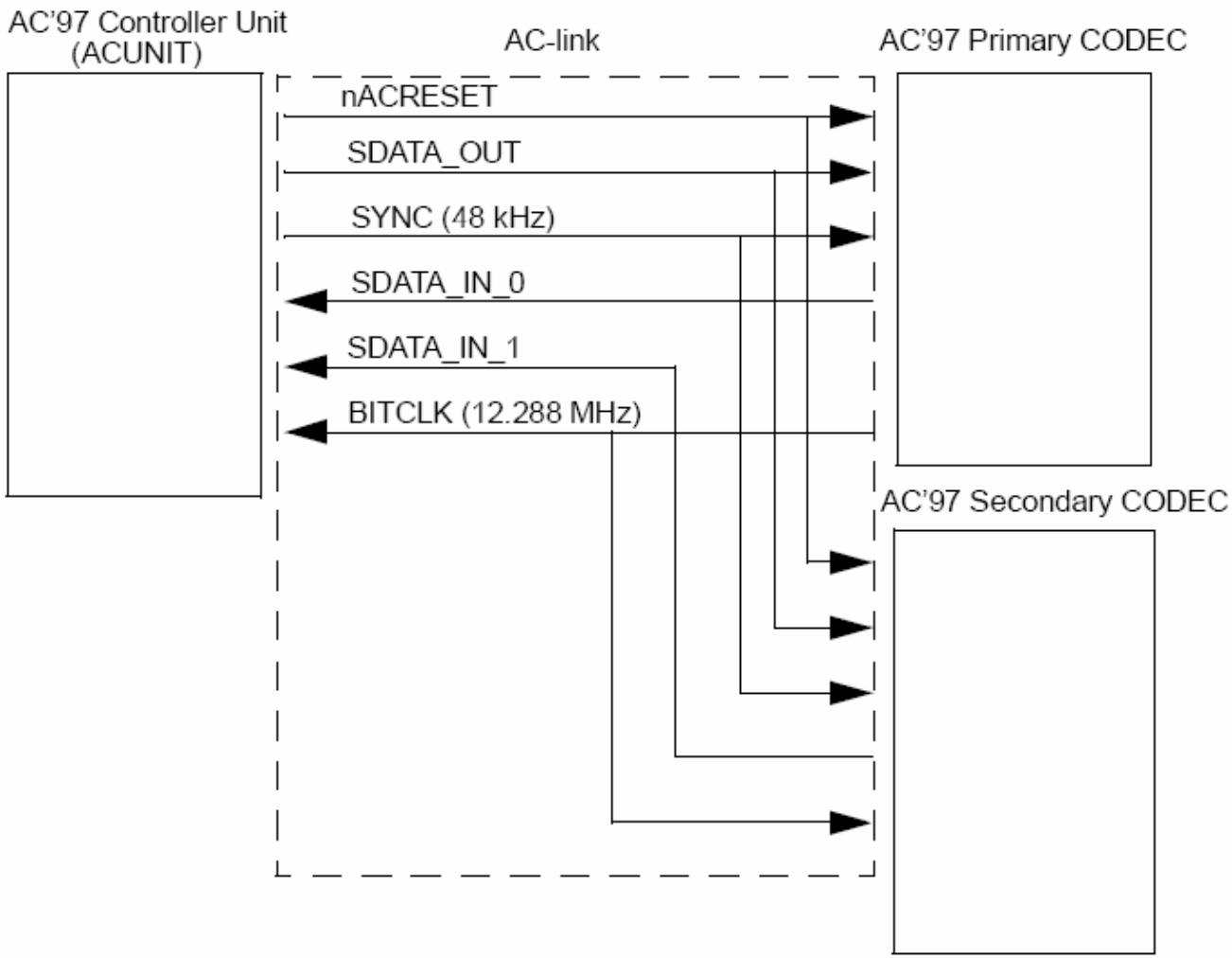
ACUNIT in Xscale (III)

- **AC-link function**
  - Point-to-point synchronous serial interconnect that supports full-duplex data transfers.
  - All digital audio streams, Modem line CODEC streams, and command/status information are communicated over the AC-link.
- **AC-link Signals**
  - The AC-link uses (shares) General Purpose I/Os (GPIOs).

Name	Direction	Description summary
nACRESET	O	Active-low CODEC reset. The CODEC's registers reset when nACRESET is asserted.
GP28/BITCLK	I	12.288 MHz bit-rate clock.
GP31/SYNC	O	48 kHz frame indicator and synchronizer.
GP30/SDATA_OUT	O	Serial audio output data to CODEC for digital-to-analog conversion.
GP29/SDATA_IN_0	I	Serial audio input data from Primary CODEC.
GP32/SDATA_IN_1	I	Serial audio input data from Secondary CODEC.

ACUNIT in Xscale (IV)

- **Data Transfer Through the AC-link**



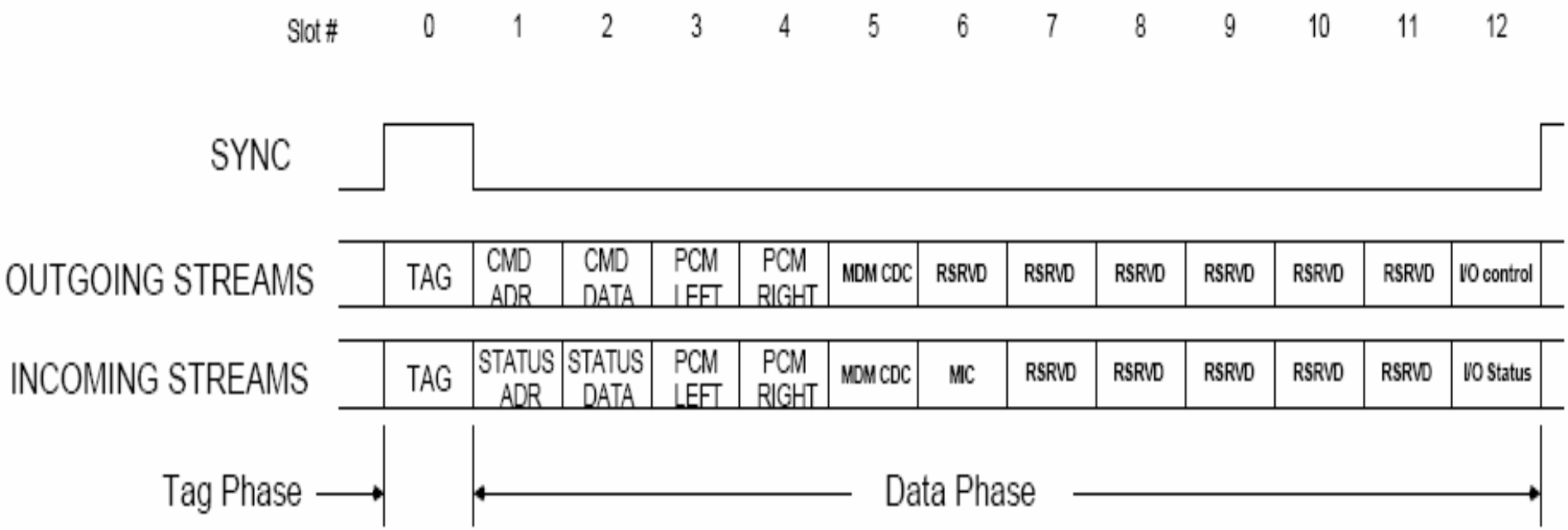
ACUNIT in Xscale (V)

- **AC97 Data Stream Formats**

Channel	Slots	Comments
PCM Playback	Two output slots	Two-channel composite PCM output stream
PCM Record data	Two input slots	Two-channel composite PCM input stream
CODEC control	Two output slots	Control register write port
CODEC status	Two input slots	Control register read port
Modem Line CODEC Output	One output slot	Modem line CODEC DAC input stream
Modem Line CODEC Input	One input slot	Modem line CODEC ADC output stream
Dedicated Microphone Input	One input slot	Dedicated microphone input stream in support of stereo AEC and other voice applications.
I/O Control	One output slot	One slot dedicated to GPOs on the modem CODEC.
I/O Status	One input slot	One slot dedicated to status from GPIs on the modem CODEC. Data is returned on every frame.

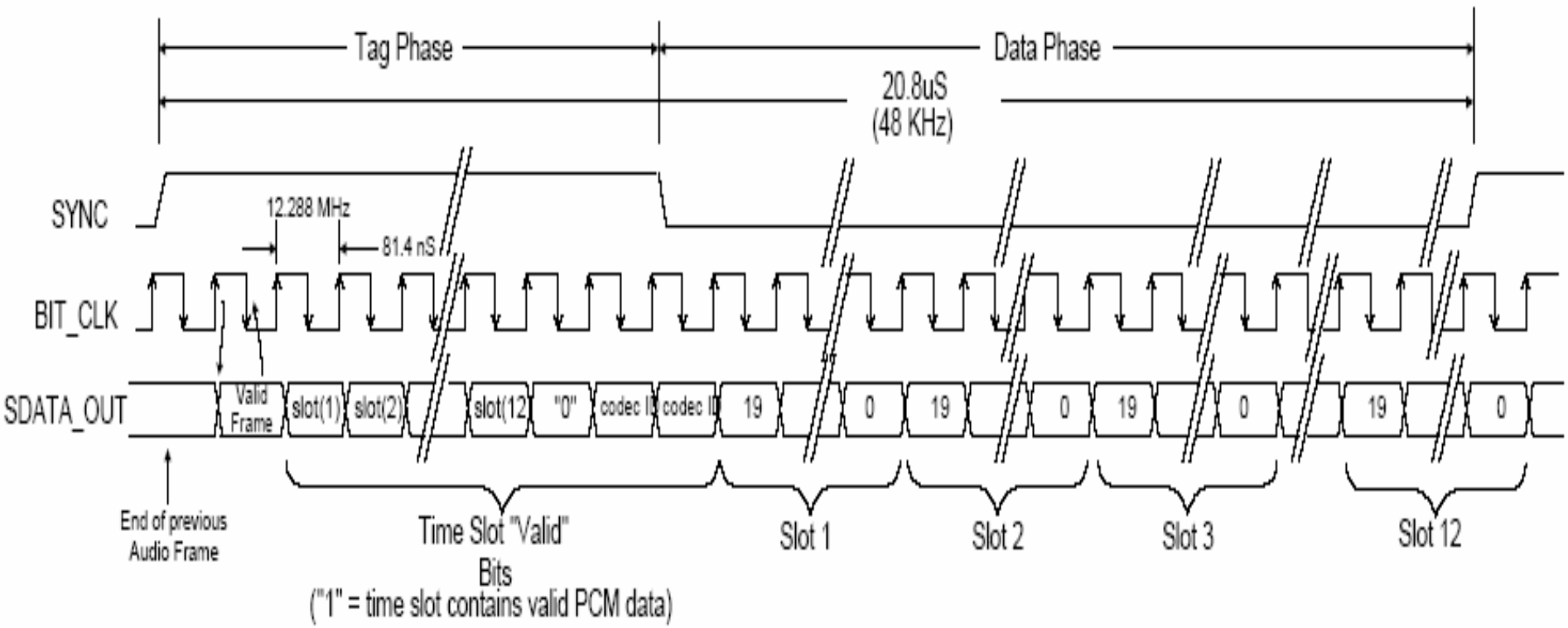
ACUNIT in Xscale (VI)

- **AC'97 Standard Bidirectional Audio Frame**
  - Slot 0 to 12 in one frame. 1/48k sec.
  - Slot 0: Tag phase. 16 bits. Sync = 1.
  - Slots 1-12: Data phase. 20 bits. Sync = 0.
  - 256 bits/frame: 12.288 MHz BITCLK.



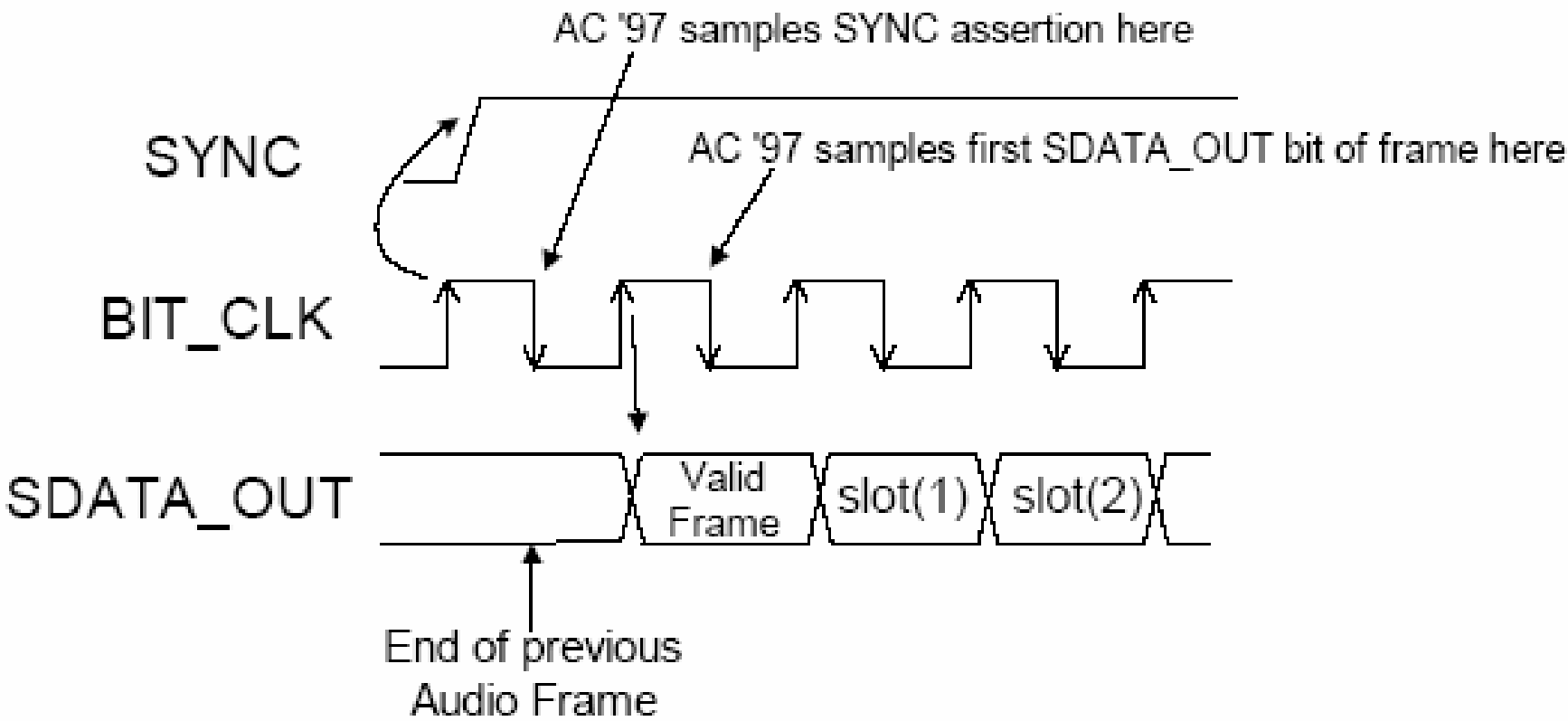
ACUNIT in Xscale (VII)

- **AC-link Audio Output Frame**
  - Multiplexed bundle of audio output data, control, etc.
  - SDATA_OUT line

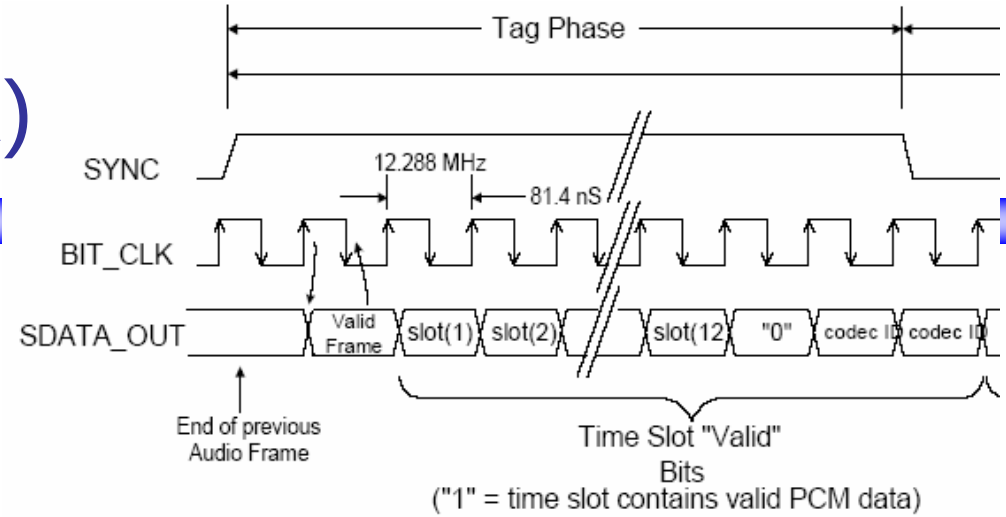


ACUNIT in Xscale (VIII)

- **Timing for start of a frame**



ACUNIT in Xscale (IX)



- **Slot 0: Tag Phase**
  - 16 bits total
  - The first bit: a global bit (SDATA_OUT slot 0, bit 15) that flags the validity for the entire audio frame.
    - If the valid frame bit is a 1, the current audio frame contains at least one slot time of valid data.
  - The next 12 bit positions sampled by AC'97 indicate which of the corresponding 12 time slots contain valid data.
  - Bits 0 and 1 of slot 0 are used as CODEC ID bits for I/O reads and writes to the CODEC registers.

ACUNIT in Xscale (X)

- **Slot 1: Command Address Port**
  - 20 bits total
  - Controls features and monitors status for AC'97 functions including mixer settings and power management.
  - Supports up to sixty-four 16-bit read/write registers, addressable on even byte boundaries.
    - Only accesses to even registers (0x00, 0x02, etc.) are valid.
  - Read: Max 4 frames to respond.
  - Slot 1 bit def. ->

Bit	Name	Description
Bit(19)	RW	1 = read, 0 = write
Bit(18:12)	IDX	Code register index
Bit(11:0)	reserved	Stuff with 0s

ACUNIT in Xscale (XI)

- **Slot 2: Command Data Port**
  - In conjunction with the Command Address Port of Slot 1.
  - WRITE:
    - Delivers 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by slot 1, bit 19).
  - READ:
    - If the current command port operation is a read, the ACUNIT fills Slot 2 with zeroes.

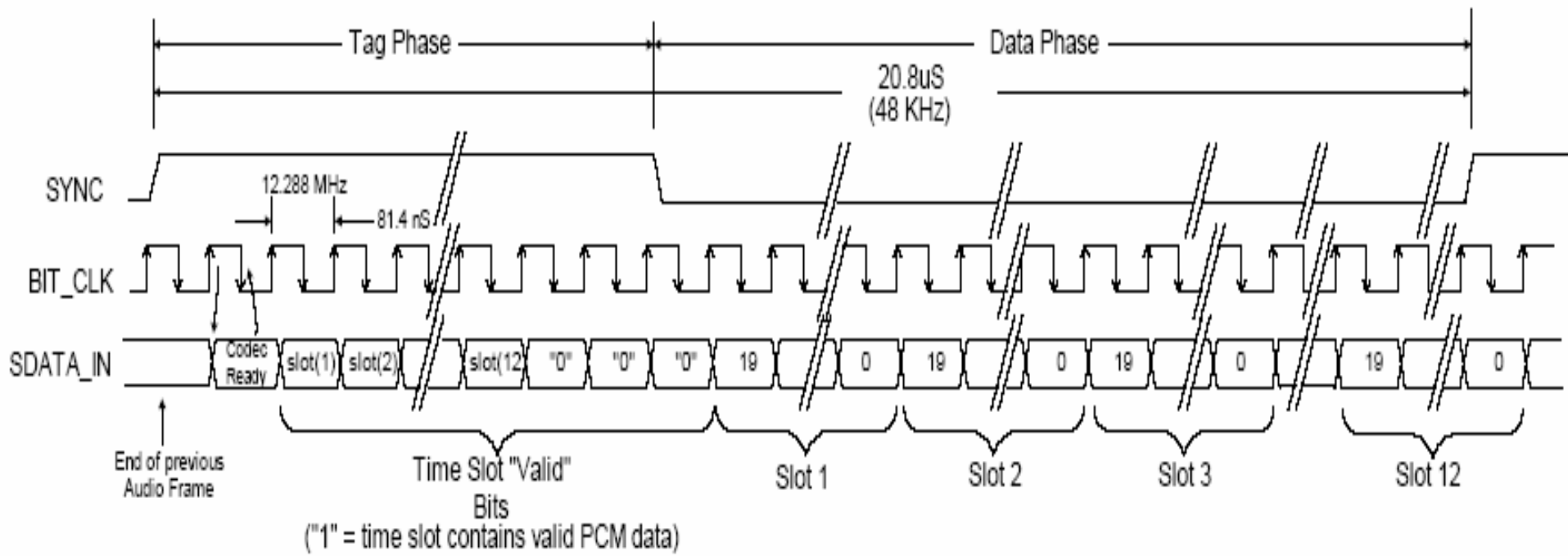
Bit	Name	Description
Bit(19:4)	Control register write data	Stuffed with 0s if current operation is a read
Bit(3:0)	reserved	Stuffed with 0s

ACUNIT in Xscale (XII)

- **Slot 3: PCM Playback Left Channel**
  - Contains the composite digital audio left playback stream.
  - If the playback stream contains an audio sample with a resolution that is less than 20 bits, the ACUNIT fills all trailing non-valid bit positions with zeroes.
- **Slot 4: PCM Playback Right Channel**
  - The composite digital audio right playback stream.
- **Slot 5: Modem Line CODEC**
  - MSB justified modem DAC input data if the modem line CODEC is supported.
- **Slots 6-11: Reserved**
  - Reserved for future use. The ACUNIT fills them with zeroes.
- **Slot 12: I/O Control**
  - Contains 16 MSB bits for GPO Status (output).

ACUNIT in Xscale (XIII)

- **AC'97 Input Frame**
  - Two SDATA_IN lines: Primary/secondary CODECs



ACUNIT in Xscale (XIV)

AC'97 Input Slots

- Slot 0: Tag phase
- Slot 1: Status Address Ports
- Slot 2: Status Data Port
- Slot 3: PCM Record Left Channel
- Slot 4: PCM Record Right Channel
- Slot 5: Optional Modem Line CODEC
- Slot 6: Optional Dedicated Microphone Record Data
- Slots 7-11: Reserved
- Slot 12: I/O Status

ACUNIT in Xscale (XV)

- **Initialization**
  - The AC'97 CODEC and ACUNIT are reset on power up.
  - To initialize the ACUNIT follow theses steps:
    - 1. Program the GPIO Direction register and GPIO Alternate Function Select register to assign proper pin directions for the ACUNIT ports.
    - 2. Set the COLD_RST bit of the GCR to one to deassert nACRESET.
      - a. Frames filled with zeroes are transmitted because the transmit FIFO is still empty. This situation does not cause an error condition.
      - b. The ACUNIT records zeroes until the CODEC sends valid data.
      - c. DMA requests are enabled.
    - 3. Enable the Primary Ready Interrupt Enable and/or the Secondary Ready Interrupt Enable by setting the PRIRDY_IEN bit and/or the SECRDY_IEN bit of the GCR to one.
    - 4. Software enables DMA operation in response to primary and secondary ready interrupts.
    - 5. The ACUNIT triggers transmit DMA requests. The DMA fills the transmit FIFO in response.
    - 6. The ACUNIT continues to transmit zeroes until the transmit FIFO is half full. When it is half full, valid transmit FIFO data is sent across the AC-link.

ACUNIT in Xscale (XVI)

- AC97 Register summary

Address	Name	Description
0x4050_0000	POCR	PCM Out Control Register
0x4050_0004	PICR	PCM In Control Register
0x4050_0008	MCCR	Mic In Control Register
0x4050_000C	GCR	Global Control Register
0x4050_0010	POSR	PCM Out Status Register
0x4050_0014	PISR	PCM In Status Register
0x4050_0018	MCSR	Mic-In Status Register
0x4050_001C	GSR	Global Status Register
0x4050_0020	CAR	CODEC Access Register
0x4050_0024 - 0x4050_003C	—	reserved
0x4050_0040	PCDR	PCM FIFO Data Register
0x4050_0044 - 0x4050_005C	—	reserved
0x4050_0060	MCDR	Mic-in FIFO Data Register
0x4050_0064 - 0x4050_00FC	—	reserved

ACUNIT in Xscale (XVII)

Address	Name	Description
0x4050_0100	MOCR	Modem-Out Control Register
0x4050_0104	—	reserved
0x4050_0108	MICR	Modem-In Control Register
0x4050_010C	—	reserved
0x4050_0110	MOSR	Modem-Out Status Register
0x4050_0114	—	reserved
0x4050_0118	MISR	Modem-In Status Register
0x4050_011C - 0x4050_013C	—	reserved
0x4050_0140	MODR	Modem FIFO Data Register
0x4050_0144 - 0x4050_01FC	—	reserved
(0x4050_0200 - 0x4050_02FC) with all in increments of 0x00004	—	Primary Audio CODEC registers
(0x4050_0300 - 0x4050_03FC) with all in increments of 0x00004	—	Secondary Audio CODEC registers
(0x4050_0400 - 0x4050_04FC) with all in increments of 0x0000_0004	—	Primary Modem CODEC registers
(0x4050_0500 - 0x4050_05FC) with all in increments of 0x00004	—	Secondary Modem CODEC registers

ACUNIT in Xscale (XVIII)

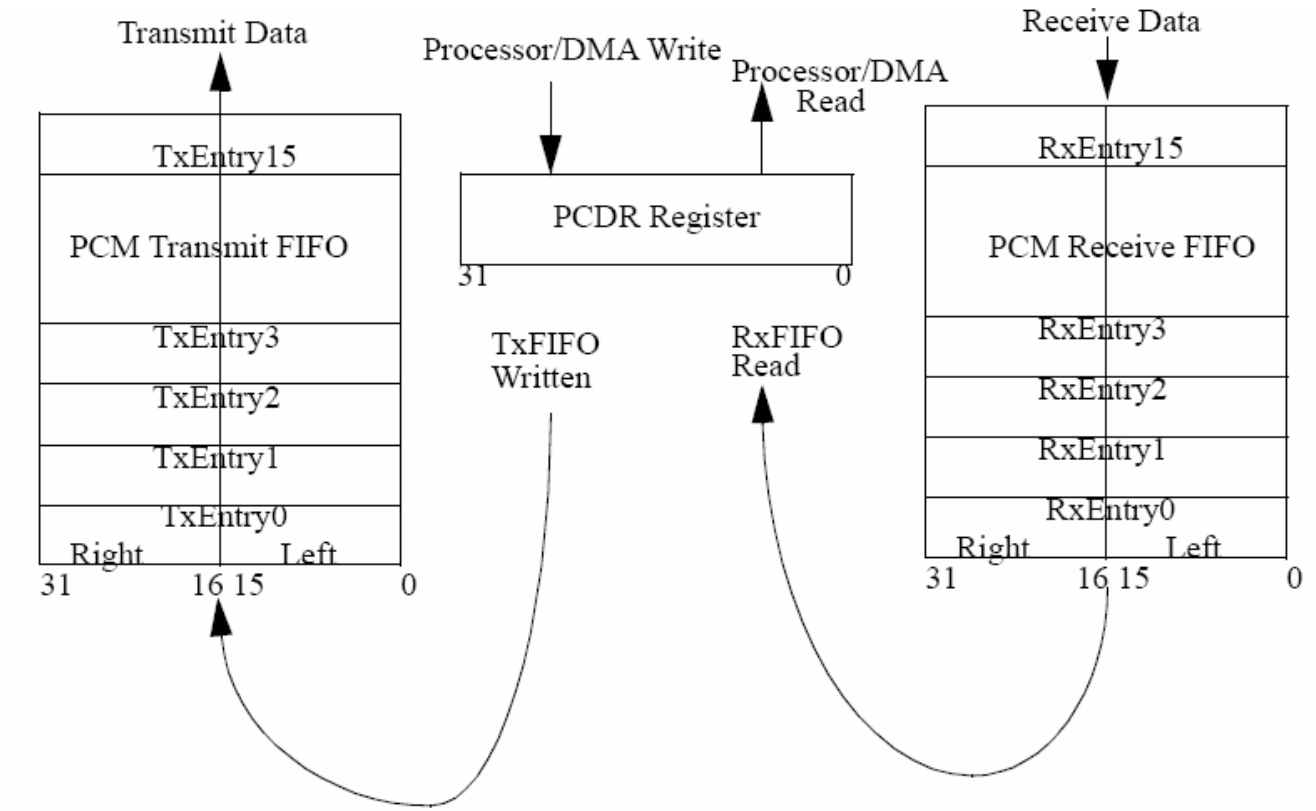
- Global Control Register (GCR)
  - Bit 19 CDONE_IE — Command Done Interrupt Enable
  - Bit 18 SDONE_IE — Status Done Interrupt Enable
  - Bit 9 SECRDY_IEN — Secondary Ready Interrupt Enable
  - Bit 8 PRIRDY_IEN — Primary Ready Interrupt Enable
  - Bit 5 SECRES_IEN — Secondary Resume Interrupt Enable
  - Bit 4 PRIRES_IEN — Primary Resume Interrupt Enable
  - Bit 3 ACLINK_OFF — AC-link shut off
  - Bit 2 WARM_RST — AC'97 Warm Reset
  - Bit 1 COLD_RST — AC'97 Cold Reset
  - Bit 0 GIE — GPI Interrupt Enable
- Global Status Register (GSR)
  - Bit 19 CDONE — Command Done
  - Bit 18 SDONE — Status Done
  - ...

ACUNIT in Xscale (XIX)

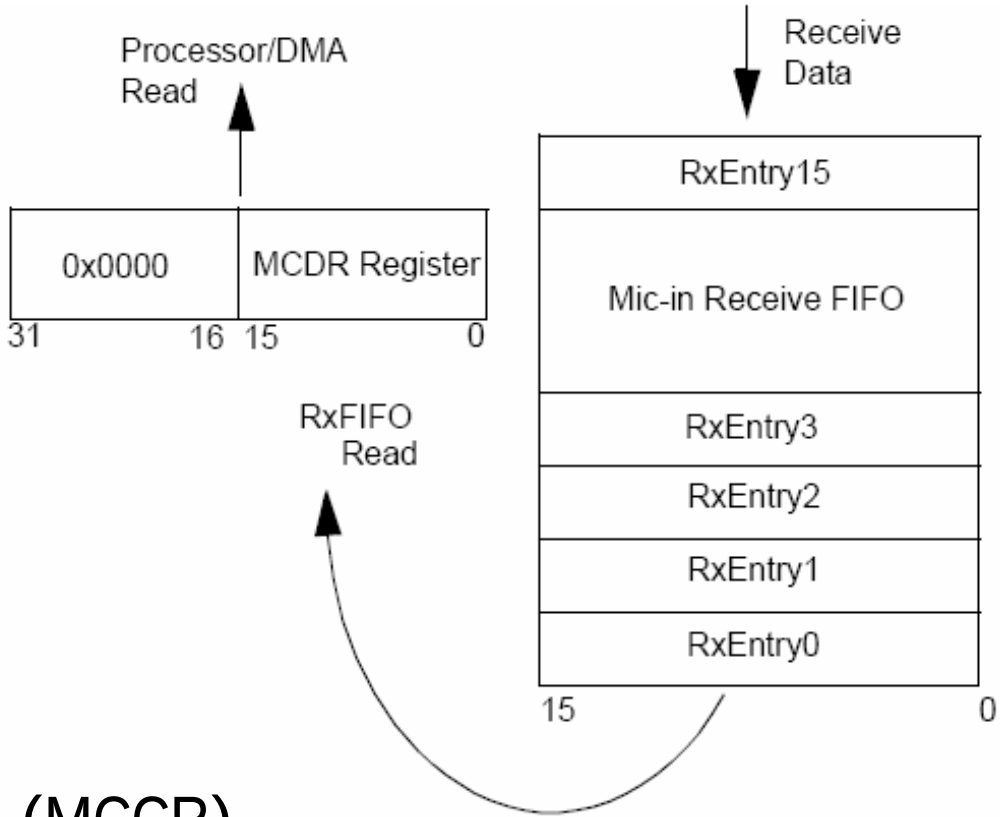
- PCM-Out Control Register (POCR)
  - Bit 3 FEIE FIFO Error Interrupt Enable
- PCM-In Control Register (PICR)
  - Bit 3 FEIE FIFO Error Interrupt Enable
- PCM-Out Status Register (POSR)
  - Bit 3 FIFOE FIFO Error
- PCM-In Status Register (PISR)
  - Bit 3 FIFOE FIFO Error
- CODEC Access Register (CAR)
  - Bit 0 CAIP CODEC Access In Progress

ACUNIT in Xscale (XX)

- PCM Data Register (PCDR)
  - Bit 31:16 PCM_RDATA PCM right channel data
  - Bit 15:0 PCM_LDATA PCM left channel data



ACUNIT in Xscale (XXI)



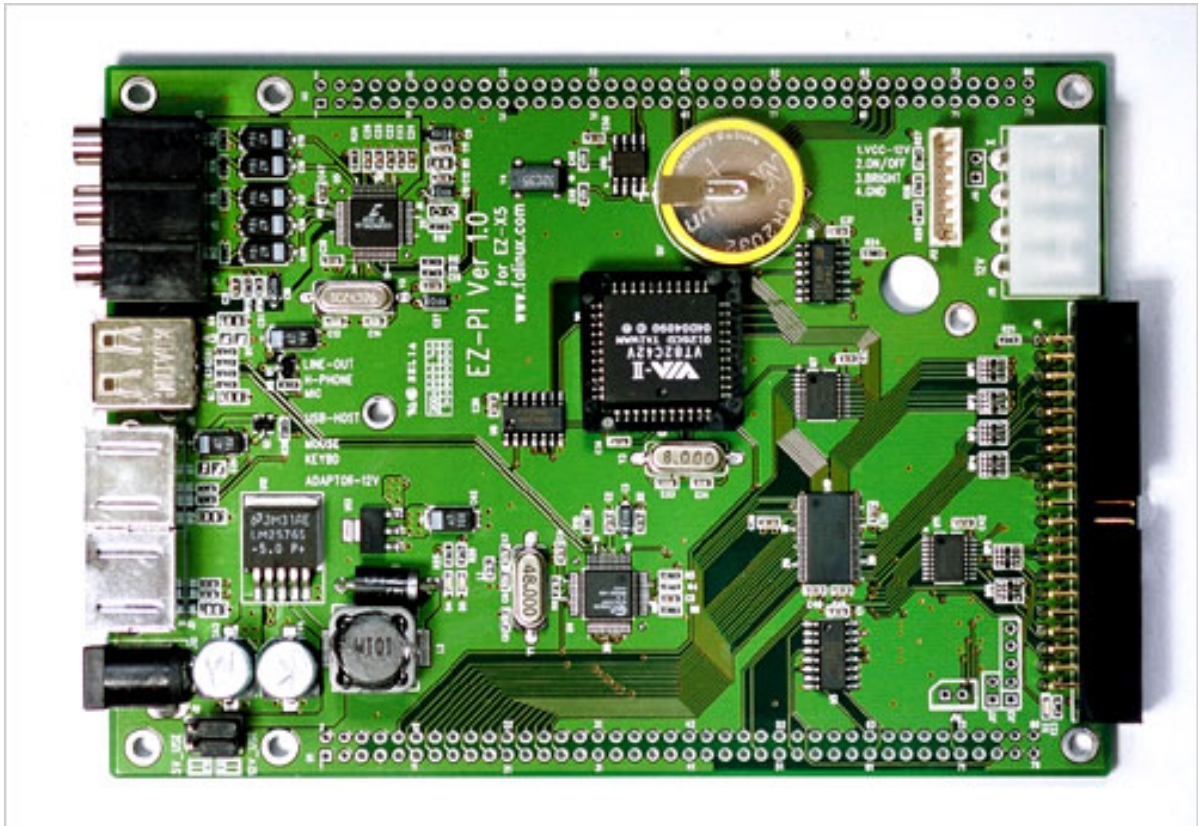
- Mic-In Control Register (MCCR)
  - Bit 3 FEIE FIFO Error Interrupt Enable
- Mic-In Status Register (MCSR)
  - Bit 3 FIFOE FIFO Error
- Mic-In Data Register (MCDR)
  - Bit 15:0 MIC_IN_DAT Mic-in data

ACUNIT in Xscale (XXII)

- Modem-Out Control Register (MOCR)
  - Bit 3 FEIE FIFO Error Interrupt Enable
- Modem-In Control Register (MICR)
  - Bit 3 FEIE FIFO Error Interrupt Enable
- Modem-Out Status Register (MOSR)
  - Bit 4 FIFOE FIFO Error
- Modem-In Status Register (MISR)
  - Bit 4 FIFOE FIFO Error
- Modem Data Register (MODR)
  - Bit 15:0 MODEM_DAT Modem data

9. EZ-X5 Audio

- **EZ-PI Board**
  - EZ-X5 **보드와 함께 사용하는 서브 보드이며** USB-Host **와** AC97 **오디오 코덱,** PS2 **키보드 및 마우스,** RTC **와** ATAPI **인터페이스가 있어** HDD**나** CD-ROM **을 장착할 수 있습니다. 그리고** TFT-LCD **백라이트용 인버터 인터페이스도 내장되어 있습니다.**



EZ-X5 Audio (II)

- **Hardware spec.**
  - **USB-Host** USB 1.1 Full Speed
  - **Audio** AC97-Codec, Head-Phone/Line-Out/MIC **지원**
  - **PS2-Port** Keyboard, Mouse **지원**
  - **IDE** HDD, CD-ROM **지원**
  - **RTC** IIC RTC **지원**

- **Software spec.**
  - **USB-Host** HID Class **등 지원**
  - **Audio** MP3, WAV Play, Recording **지원**
  - **PS2-Port** **가상터미널 지원**
  - **IDE** **다양한 파일 시스템 지원**
  - **RTC** **시간설정 지원**

EZ-X5 Audio (III)

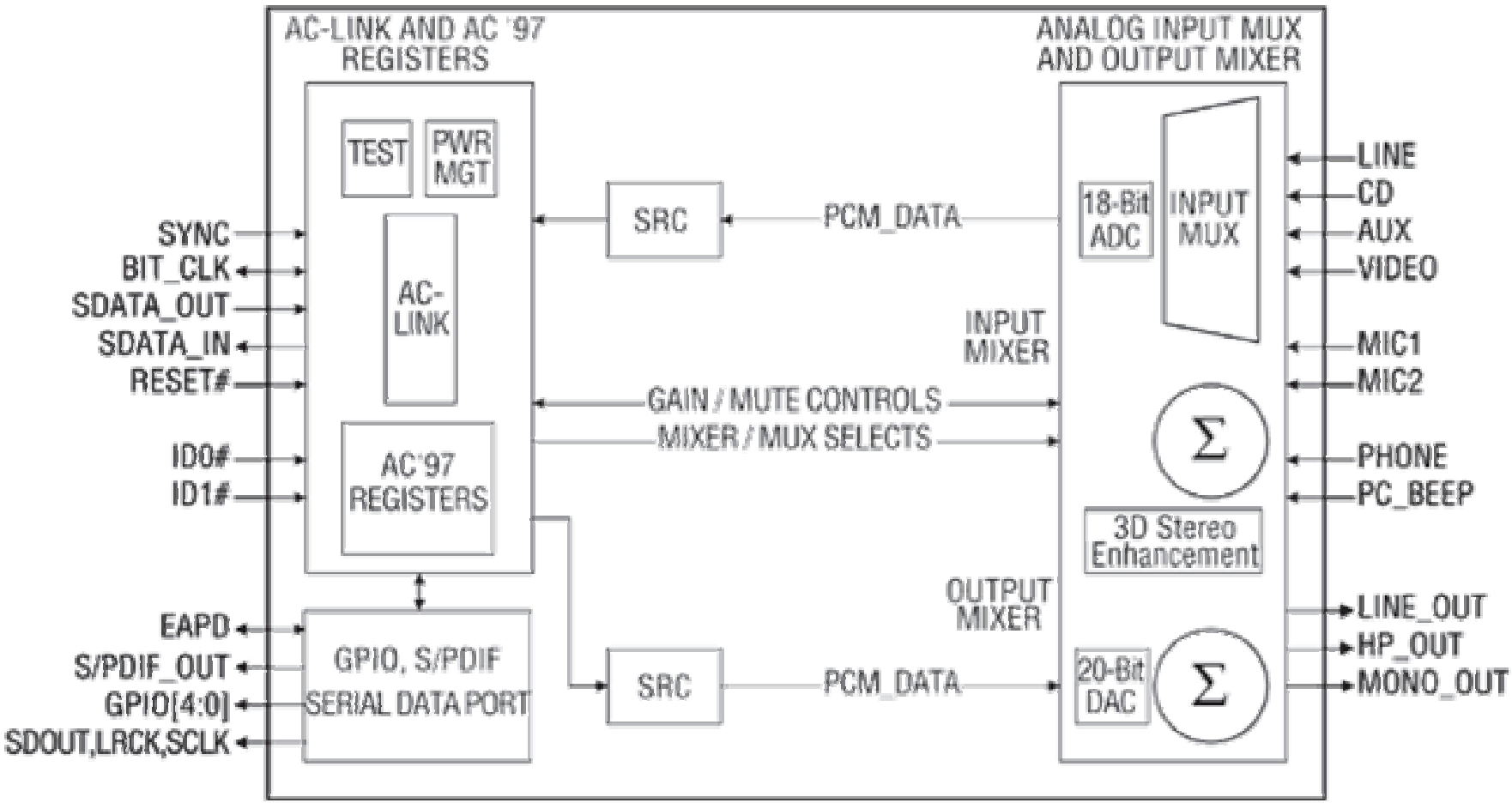
- **CS4202 Audio CODEC ’97 with Headphone Amplifier**
  - An AC '97 2.2-compliant, stereo audio CODEC designed for PC multimedia systems.
  - Uses industry-leading Delta-Sigma and mixed-signal technology.
  - Designed to help enable the design of PC 99- and PC 2001-compliant, high-quality audio systems for desktop, portable, and entertainment PCs.
  - The CS4202 includes two I²S outputs, which allow for the addition of one or two low-cost stereo digital-to-analog (D/A) converters (CS4334) for 4- or 6-channel audio.
  - Coupling the CS4202 with a PCI audio accelerator or core logic supporting the AC '97 interface implements a cost-effective, superior-quality audio solution.
  - Windows XP and 2000 drivers are available.

EZ-X5 Audio (IV)

- **Features of CS4202**
  - AC '97 2.2-compliant
  - Exceeds Microsoft PC 2001 audio requirements
  - Integrated high-performance headphone amplifier
  - On-chip PLL for use with external clock sources
  - Integrated high-performance microphone pre-amplifier
  - Automatic jack sense through general-purpose I/O
  - BIOS driver interface for audio feature configuration through software
  - 20-bit stereo D/A converter; 18-bit stereo A/D converter with sample rate converters
  - Inputs:
    - Line-level: 3 stereo and 2 mono
    - Mic-level: 2 mono
    - High-quality pseudo-differential CD input
  - Outputs:
    - S/PDIF digital audio output
    - I²S serial digital for cost-effective 6-channel apps
    - Simultaneous S/PDIF and 6-channel audio playback
    - Stereo aid mono line-level.

EZ-X5 Audio (V)

- **Block diagram of CS4202**



References

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- CS4202
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